IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: Huan nan Ma et al.

Serial No.: 10/522,057

Group Art Unit: 2416

Filed: April 25, 2005

Examiner: KAO, Wei Po Eric

For: METHOD ABOUT PROTECTING HIGH LAYER SERVICE IN THE MULTILAYER COMMUNICATION EQUIPMENT

Confirmation No.: 2070

APPEAL BRIEF

Pursuant to 37 C.F.R. § 41.37, Applicants submit this Appeal Brief in support of appeal from the decision of the Primary Examiner in the Final Office Action dated June 25, 2008, finally rejecting claims 1-5, and confirmed in the Advisory Action mailed October 29, 2008.

Applicants request that the final rejections of claims 1-5 be REVERSED with instructions to the Primary Examiner to allow the pending claims.

A Petition for Extension of Time is concurrently submitted herewith extending the time for submission of this Appeal Brief one (1) month from January 24, 2009 to February 24, 2009.

The Director is hereby authorized to charge the fee for filing this Appeal Brief, namely, $540, as well as any other fees which may be required, or credit any overpayment, to Deposit Account Number 04-1679.

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I. Real Party In Interest

The real party in interest is the ZTE Corporation, present owner of the application and the invention described therein.

II. Related Appeals and Interferences

There are no related appeals or interferences.

III. Status Of Claims

Claims 1-5 are pending in the present application. Claims 1-5 all stand rejected, and their rejection is hereby appealed.

IV. Status Of Amendments

No after-final amendments were submitted with respect to the appealed claims 1-5.

V. Summary Of Claimed Subject Matter

Applicants' invention relates to a method of protecting high layer service in multi-layer communication equipment. Page 1, lines 30-31. A low layer processing module provides low layer transmission passages for a high layer processing module. Page 1, lines 32-33; Page 3, lines 27-34; and FIG. 3. The high layer processing module sets up a transparent VP link passage from upstream and downstream nodes. *Id.* Once a fault of the processing module is detected, the high layer processing module will message the low layer processing module, and the low layer processing module will set up a bypass connection isolating the failed high layer processing module. Page 3, lines 35-40. The Applicants' invention protects ATM traffic when the processing ability of the ATM layer is invalidated between the Multi-Service Provisioning Platform (MSPP) and the Multi-Service Transport Platform (MSTP) without requiring extra network passages.

Independent claim 1 is directed to a method of protecting high layer service in multi-layer communication equipment. First, low layer processing module provides high layer processing module with low layer transmission passage. Page 1, lines 32-33; Page 3, lines 27-34; and FIG. 3. Second, high layer processing module extract and insert high layer service of the multi-layer communication equipment from low layer transmission passage, avoiding changing the service between upstream node and downstream node after passing high layer processing module of the multi-layer communication equipment. Page 1, lines 34-38; page 3, lines 18-24; and FIG. 3. Third, after high layer processing module detecting said high layer processing module encountering a trouble, it will inform low layer processing module. Page 1, lines 39-40; FIG. 4. Fourth, a bypass will be set up after low layer processing module detecting high layer processing module encountering the trouble, so as to isolate the high layer processing module encountering a trouble. Page 1, line 41 to page 2, line 1; page 3, lines 35-40; and FIG. 4.

Dependent claim 2 recites additional features of the second step of claim 1. Specifically, claim 2 discloses that in the second step of claim 1, a transparent virtual path connection is set up for the service passing the high layer processing module of the node, namely for ATM traffic. Page 3, lines 27-29; FIG. 3. A cross connection, which changes neither virtual path identification nor virtual channel identification, is set up to avoid changing the service between upstream node and downstream node after passing high layer processing module of the said node. Page 3, lines 29-40; FIG. 4.

Dependent claim 4 recites additional features of the fourth step of claim 1. Specifically, claim 4 discloses that in the fourth step, the low layer processing module judges whether the service signal that is transmitted by the high layer processing module is invalid, or by detecting hardware signals or software messages sent by high layer processing module indicating that it is invalid. Page 2, lines 2-6.

VI. Grounds Of Rejection To Be Reviewed On Appeal

1. Whether the differences between claims 1-5, rejected by the Examiner under 35 U.S.C. § 103(a), and U.S. Patent Application Publication No. 2002/0162045 in the name of Shiragaki ("Shiragaki") in combination with U.S. Patent Application

Publication No. 2001/0046206 in the name of Chan et al. ("Chan"), are such that the subject matter claimed as a whole would have been obvious to a person of ordinary skill in the art at the time of the invention.

VII. Argument

A. Claims 1-5 are patentable over the Examiner's proposed combination of Shiragaki and Chan under 35 U.S.C. § 103(a) because Examiner failed to establish a *prima facie* case of obviousness.

Claims 1-5 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Shiragaki in view of Chan. *See* Office Action mailed June 25, 2008, page 7. Under 35 U.S.C. § 103(a), a claim is unpatentable for obviousness when the "subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains." The Patent Office "has the burden of showing a *prima facie* case of obviousness." *In re Mayne*, 104 F.3d 1339, 1341 (Fed. Cir. 1997); *In re Sullivan*, 84 USPQ2d 1034, 1038 (Fed. Cir. 2007).

Whether the subject matter of a claim is obviousness is based on the following factual inquiries: (1) the scope and content of the prior art; (2) the level of ordinary skill in the art; (3) the differences between the prior art and the claimed invention; and (4) the extent of any objective indicia of non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). The Supreme Court more recently held that the four Graham factors "continue to define the inquiry that controls" under 35 U.S.C. § 103. *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1734, 82 USPQ2d 1385, 1391 (2007).

The Final Office Action fails to address each of the four factual inquiries mandated by the United States Supreme Court in *Graham* for determining whether a claimed invention is obvious under 35 U.S.C. § 103. Importantly, the third listed *Graham* factor requires "resolving the level of ordinary skill in the pertinent art." 383 U.S. at 17-18. Nowhere within the Final Office Action, or within the entire prosecution history, does the Examiner ever resolve, or even attempt to resolve, the level of ordinary skill in the pertinent art. The Final Office Action is silent on this issue - ignoring this

factor, rather than resolving it, as mandated by the Supreme Court. *See* Final Office Action mailed June 25, 2008, pages 7-10.

By failing to resolve the level of ordinary skill in the art, the Examiner has failed to meet his burden of showing a *prima facie* case of obviousness for all claims rejected under Section 103 since a *prima facie* case of obviousness cannot be established by failing to address all of the *Graham* factors. Moreover, errors in resolving the level of ordinary skill in the art when evaluating obviousness are reversible. *Daiichi Sankyo Co. v. Apotex Inc.*, 84 USPQ2d 1285, 1287 (Fed. Cir. 2007) ("The district court's error in determining the level of ordinary skill in the art of the '741 patent tainted its obviousness analysis"). By failing to address this critical obviousness factor, the Final Office Action prevents Applicants from determining whether the Patent Office has committed reversible error in its obviousness analysis. Accordingly, Applicants are deprived of their due process right to respond to an obviousness rejection based upon all of the factual inquiries mandated by the Supreme Court in *Graham* and in *KSR*.

Accordingly, the Examiner's rejection of the subject claims based upon the proposed combination of the Shiragaki and Chan references are invalid and should be reversed since the Examiner failed to establish a *prima facie* case of obviousness.

B. Claims 1-5 are patentable over the Examiner's proposed combination of Shiragaki and Chan under 35 U.S.C. § 103(a) because the proposed combination does not teach or suggest every feature of independent claim 1 including "a bypass will be set up after low layer processing module detecting high layer processing module encountering the trouble, so as to isolate the high layer processing module encountering a trouble."

Claim 1 has been rejected by the Examiner as allegedly being unpatentable under 35 U.S.C. § 103(a) over a proposed combination of the Shiragaki reference and the Chan reference. *See* Office Action mailed June 25, 2008, page 7. Even if one assumes that the Examiner had met his burden of resolving the level of skill in the art, a burden that Applicants vehemently deny has been met, the Examiner's rejection of these claims would still be arbitrary and capricious as one skilled in the art would not have combined the references to provide a method as recited in claim 1.

The Examiner attempts to invent a rejection by alleging that Shiragaki and Chan disclose a method of protecting high layer service in multi-layer communication equipment in which a bypass will be set up after a low layer processing module detects a high layer processing module encounters a trouble, so as to isolate the high layer processing module encountering the trouble. Because the proposed combination of Shiragaki and Chan does not include or suggest all of the limitations of the subject claims, and since the method of protecting high layer service in multi-layer communication equipment would not have been obvious to one skilled in the art the time the invention was made, the Examiner's rejections on this basis are invalid and should be reversed.

Claim 1 recites that "a bypass will be set up after low layer processing module detecting high layer processing module encountering the trouble, so as to isolate the high layer processing module encountering a trouble." On page 7 of the Final Office Action, the Examiner alleges that Shiragaki discloses this claimed feature.

Shiragaki discloses a communication device having an automatic failure recovery function consisting of an A layer communication unit 107 and a B layer communication unit 108. Paragraph [0164]. The A and B layers notify each other if a failure has occurred in one or more of the layers and failure recovery has been initiated through the failure recovery information communication terminal and processing units 103, 104. Paragraphs [0168] and [0172].

When a failure occurs in multiple layers of the Shiragaki device, the A layer failure detection and recovery processing unit 101 and the B layer failure detection and recovery processing unit 102 are activated simultaneously but individually. Paragraph [0171]. The first layer reach the stage immediately before the switching of a main signal notifies the other layer through the inter layer failure recovery information communication terminal and processing units 103, 104 to stop the failure recovery in the other layer. Paragraph [0172]. The other layer will then send back a response through the failure recovery information communication terminal and processing units 103, 104 to notify the first layer that the main signal may then be switched. Paragraph [0173]. However, if a response message is not received from the other layer within a preset

period of time, then an interrupt will occur and the first layer to complete failure recovery will seek a decision from an operator about how to proceed. Paragraph [0174].

As set forth above, the Shiragaki reference does not teach or suggest a method for protecting high layer service in a multi-layer communication equipment in which a bypass is set up after the low layer processing module detects a high layer processing module encounters the trouble, so as to isolate the high layer processing module encountering the trouble as recited in claim 1. Instead, Shiragaki discloses a system in which messages are repeatedly transmitted from one layer to another layer to determine the status of a failure recovery operation being performed in the other layers. Additionally, the layers in Shiragaki transmit reservation request and reservation acknowledgement messages to ensure that the switching of the main signal does not simultaneously occur in several layers. Accordingly, none of the layers in Shiragaki are isolated from the other layers since an interrupt in which the device requests intervention from an operator occurs if a response message is not received from one of the layers after a preset period of time. Thus, the system in Shiragaki does not isolate a layer upon detection of a failure, but instead uses an interlayer messaging system through which multiple messages are transmitted to coordinate the switching of the main signal to ensure that system instability caused from multiple layers simultaneously switching is avoided.

The Chan reference does not cure the deficiencies of Shiragaki with respect to the claimed feature of setting up a bypass after the low layer processing module detects high layer processing module encounters a trouble, so as to isolate the high layer processing module encountering a trouble. Chan discloses a SONET VPR protection method and apparatus including a plurality of Time Division Add Drop Multiplexers (ADMs) and a plurality of Distributed Access Switches (DAS). Paragraph [0051]. Each DAS includes a SONET_N card 130, a SONET_S card 132, two Line Cards 134, 136, and an electronic switch 138. *Id.*

Chan also discloses an Intra-Ring Communication (IRC) Protocol through which SONET nodes may be added or deleted from a ring, and a ring failure is communicated to other SONET nodes and to all line cards of the SONET nodes. Paragraph [0057]. If a failure is detected by a SONET node, then according to the IRC Protocol, a failure

message is sent from the detecting SONET node in both upstream and downstream directions relative to the detecting SONET node (e.g., clockwise and counterclockwise along the ring). Paragraph [0064]. The detecting node's identification and failure detection are used by a protection switch mechanism to reroute the cells around the failure by either updating look-up tables (LUTs) or retrieving alternative Virtual Path Identifiers (VPIs) and Virtual Channel Identifiers (VCIs) from a Destination Protection Table 425. Paragraphs [0064], [0066], [0069], and [0070].

Nowhere within the entirety of Chan is it taught or suggested that a low layer sets up a bypass after detecting a high layer processing module encounters a trouble so as to isolate the high layer processing module. Thus, Chan fails to cure the deficiencies of Shiragaki with respect to a low layer setting up a bypass after detecting the high layer processing module encountering a trouble, so as to isolate the high layer processing module encountering a trouble as recited in claim 1.

Regardless of the fact that neither Shiragaki nor Chan teach or suggest that a low layer setting up a bypass after detecting the high layer processing module encountering a trouble, so as to isolate the high layer processing module encountering a trouble, the Examiner alleges that claim 1 would have been obvious to one ordinary skill in the art without having ever resolved what the level of one or ordinary skill in the art. Significantly, without knowing what the level of skill in the art was at the time the invention was made, the only facts of record pertaining to the level of skill in the art are found within the prior art of record, i.e., Shiragaki and Chan. As set forth above, neither Shiragaki nor Chan teach or suggest a low layer setting up a bypass after detecting the high layer processing module encountering a trouble, so as to isolate the high layer processing module encountering a trouble.

Accordingly, one skilled in the art would not have been motivated to develop a method as recited in claim 1, but instead one skilled in the art would have developed a method in which failure recovery processing units disposed in a plurality of layers repeatedly communicate with each other when a failure occurs and to coordinate when a switch should occur as disclosed in Shiragaki, or one skilled in the art would have implemented an IRC Protocol in which a failure message is used to calculate or retrieve new VPIs and VCIs for a cell as disclosed in Chan. Thus, the Examiner's failure to

resolve the level of ordinary skill in the art has resulted in the Examiner losing objectivity in determining the patentability of claim 1. *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718, 21 USPQ2d 1053, 1057 (Fed. Cir. 1991). The Examiner's rejection under 35 U.S.C. § 103(a) is not proper and should be reversed.

Regarding the Examiner's rejection of dependent claims 2-5, these rejections cannot stand because claims 2-5 depend from claim 1, which, as explained above, is allowable. *See, e.g., In re Fine*, 837 F.2d 1071, 1076 (Fed. Cir. 1988) ("Dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious."); *accord Hartness Int'l, Inc. v. Simplimatic Eng'g Co.*, 819 F.2d 1100, 1108, 2 USPQ2d 1826, 1831 (Fed. Cir. 1987); *In re Abele*, 684 F.2d 902, 910, 214 USPQ 682, 689 (CCPA 1982); *cf.* 37 C.F.R. § 1.75 ("Claims in dependent form shall be construed to include all the limitations of the claim incorporated by reference into the dependent claim."). Consequently, the Examiner's separate rejection of the subject claims based on the proposed combination of the Shiragaki and Chan references are invalid and should be reversed.

C. Claim 2 is separately patentable over the Examiner's proposed combination of Shiragaki and Chan under 35 U.S.C. § 103(a) because the proposed combination does not teach or suggest every feature of dependent claim 2, including "a cross connection, which changes neither virtual path identification nor virtual channel identification, will be set up, to avoid changing the service between upstream node and downstream node after passing high layer processing module of the said node."

Claim 2 stands rejected under 35 U.S.C. § 103(a) over Shiragaki and Chan. Office Action mailed June 25, 2008, page 9. The Examiner alleges that paragraphs [0015-0016], [0018], [0020], and [0022-0023] in Chan disclose the features recited in claim 2. *Id.*

When determining the differences between the prior art and the claimed invention, a prior art reference must be considered in its entirety including portions that would lead away from the claimed invention." MPEP § 2141.02(VI) citing *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). The Supreme Court has recently held that when the prior

art teaches away from a combination, then the combination is likely to be nonobvious. *KSR*, 127 S.Ct at 1740.

As set forth above section VII(B), Shiragaki discloses a communication device having an automatic failure recovery function consisting of an A layer communication unit 107 and a B layer communication unit 108 for an IP layer and an optical path layer. Paragraph [0164]. Shiragaki does not teach or suggest a transparent virtual path being setup that creates a cross connection that changes neither virtual path identification nor virtual channel identification as these layer are not included in an IP communication system.

The Chan reference fails to cure the deficiencies of Shiragaki with respect to a transparent virtual path connection, a cross-connection, being set up for the service passing the high layer processing module of the node, namely ATM traffic, which changes neither the virtual path identification nor virtual channel identification as recited in claim 2 as Chan explicitly teaches away from this claimed feature. The paragraphs in Chan relied upon by the Examiner describe the features of a conventional ATM system. Specifically, the paragraphs relied upon by the Examiner disclose that the cell header of a ATM cell includes Virtual Path Identifiers (VPI) and Virtual Channel Identifiers (VCI). Paragraph [0015]. Additionally, these passages disclose that two levels of routing hierarchies, Virtual Paths (VPs) and Virtual Channels (VCs), are defined for ATM traffic by using routing tables that are stored at each node, and that a VP is a collection of one or more VCs traversing multiple nodes. *Id.*

As set forth above in Section VII(B), Chan's application is directed to a protocol for ATM over SONET that may be used to add and drop SONET nodes from the network ring as well as to communicate ring failures to all line cards and all SONET nodes on the ring. Paragraph [0058]. Chan discloses two ways in which a protection switch is performed after a failure notification is detected in the SONET ring. The first method of performing a protection switch is as follows:

> "Once the SONET nodes have been notified of a failure via the IRC protocol, a protection switch is performed. The most conceptually straightforward way to perform protection switching would be to sequentially update the [look up table (LUTs)] contents for all affected VPs. That is, once notified of failure, the SONET nodes would determine which VPs are

> affected and then update the LUTs." Paragraph [0066] (emphasis added).

Accordingly, Chan's first method of performing a protection switch changes the VPI/VCI of a cell by having each SONET node update a look-up table thereby changing the channel through which the cell is transmitted when a failure is detected.

Chan's second method of performing a protection switch includes a Protection Switch Block that removes the first four octets of each ATM cell header including the Virtual Path Identifier (VPI). Paragraph [0068]. The Protection Switch Block then uses the VPI field to access an external memory that includes a Destination Protection Table. Paragraph [0069]. The Destination Protection Table includes an Alternate VPI field, which is used as a replacement VPI in the event that the preferred route is blocked due to a ring failure. *Id.* Thus, both of Chan's proposed methods of performing a protection switch change the VPI of a cell thereby explicitly teaching away from the method recited in claim 2.

Therefore, one skilled in the art would not be motivated by Shiragaki and Chan to provide a method for protecting high layer service in a multi-layer communication equipment as recited in claim 2, but instead would be motivated to change the service between upstream nodes and downstream nodes as explicitly taught by Chan. As the references teach away from the method recited in claim 2, the Examiner's rejection of claim 2 is invalid and should be reversed.

D. Claim 4 is separately patentable over the Examiner's proposed combination of Shiragaki and Chan under 35 U.S.C. § 103(a) because the proposed combination does not teach or suggest every feature of dependent claim 4, including a "wherein in the fourth step, said situation that low layer processing module detect high layer processing module encountering trouble further comprising: low layer processing module judges whether the service signal transmitting by high layer processing module is invalid or not".

Claim 4 also recites features that are not disclosed or suggested by Shiragaki and Chan. Specifically, claim 4 discloses that "in the fourth step, the situation that low layer processing module detect high layer processing module encountering trouble

further comprising: low layer processing module judges whether the service signal transmitting by high layer processing module is invalid or not...."

In rejecting claim 4, the Examiner again fails to resolve the level of skill in the art and merely cites, without explanation, FIG. 3 and paragraph [0186] of Shiragaki in support of the rejection. *See* Final Office Action, page 10. The Federal Circuit has held that "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006). *See also KSR*, 127 S.Ct at 1741 (quoting Federal Circuit statement with approval).

Paragraph [0186] of Shiragaki discloses that "[t]he A layer that received the path reservation notice 207 stops the failure recovery operation at that stage, and releases the path or the like which have been reserved until now." Nowhere within paragraph [0186] or the entirety of Shiragaki is it taught or even suggested that the low layer processing module detects the high layer processing module encounters a trouble by judging whether the service signal transmitting by high layer processing module is invalid or not. Chan also fails to teach or suggest that a low layer processing module detect a high layer processing module encountering a trouble by judging whether the service signal transmitted by high layer processing module is invalid or not.

As neither reference teaches or suggests suggested that the low layer processing module detects the high layer processing module encounters a trouble by judging whether the service signal transmitting by high layer processing module is invalid or not, one skilled in the art at the time of the invention would not have developed a method as recited in claim 4.

Accordingly, the Examiner's conclusory rejection of claim 4 under 35 U.S.C § 103(a) based on an unarticulated combination of Shiragaki and Chan without having resolved the level of ordinary skill in the art cannot stand. The Examiner's rejection of claim 4 should be reversed.

VIII. Conclusion

For the reasons stated above, the Examiner's rejections of claims 1-5 are erroneous. The rejections based on 35 U.S.C. § 103(a) are invalid because, among other reasons, (i) the Examiner has failed to consider each and everyone of the Graham factors as required for the determination of obviousness, and (ii) none of the references relied upon by the Examiner discloses a bypass will be set up after low layer processing module detecting high layer processing module encountering the trouble, so as to isolate the high layer processing module encountering a trouble. The prior art does not meet the invention claimed as a whole. Consequently, the Examiner's rejections of the pending claims based upon the prior art of record in this case are without merit and should be reversed.

Applicant submits that this application is in condition for allowance and respectfully requests reversal of all rejections of the claims and remand to the Examiner with instructions to process the application for allowance.

Dated: 2/24/09

Respectfully submitted,

/Samuel W. Apicelli/

Samuel W. Apicelli
Reg. No. 36,427
Duane Morris LLP
30 South 17th Street
Philadelphia, PA 19103-4196
tel. 215-979-1255
fax. 215-689-0827
swapicelli@duanemorris.com

Docket No. E1734-00007

Claims Appendix

1. A method for protecting high layer service in a multi-layer communication equipment, comprising the following process:

First, low layer processing module provides high layer processing module with low layer transmission passage;

Second, high layer processing module extract and insert high layer service of the multi-layer communication equipment from low layer transmission passage, avoiding changing the service between upstream node and downstream node after passing high layer processing module of the multi-layer communication equipment;

Third, after high layer processing module detecting said high layer processing module encountering a trouble, it will inform low layer processing module;

Fourth, a bypass will be set up after low layer processing module detecting high layer processing module encountering the trouble, so as to isolate the high layer processing module encountering a trouble.

2. A method for protecting high layer service in a multi-layer communication equipment according to claim 1, wherein in the second step, a transparent virtual path connection is set up for the service passing the high layer processing module of the said node, namely for ATM traffic, a cross connection, which changes neither virtual path identification nor virtual channel identification, will be set up, to avoid changing the service between upstream node and downstream node after passing high layer processing module of the said node.

3. A method for protecting high layer service in a multi-layer communication equipment according to claim 1, wherein in the third step, when high layer processing module detects the said module encountering trouble, it will inform low layer processing module by soft messages or hardware signals.

4. A method for protecting high layer service in a multi-layer communication equipment according to claim 1, wherein in the fourth step, said situation that low layer

processing module detect high layer processing module encountering trouble further comprising: low layer processing module judges whether the service signal transmitting by high layer processing module is invalid or not, or low layer processing module detects the hardware signals or soft messages sending by high layer processing module indicating its invalidation.

5. A method for protecting high layer service in a multi-layer communication equipment according to claim 1 or 4, wherein said bypass connection is actual connection of the physical lines, or it is logical connection within low layer processing module.

Evidence Appendix

NONE

Related Proceedings Appendix

NONE